FUNCTION

Incremental encoder

VHDL File

Encdig3w.vhd

Applicable Devices

Spartan 3A DSP, Spartan 6, Kintex 7, Zynq

Xilinx primitive used

DSP48A

Sub modules used

Idivision.vhd
dsp48a4m.vhd

Execution time

42 clock cycles

Introduction

The Incremental Encoder IP core provides elaboration for the raw signals received from an incremental encoder. The output is the electric angle. It is provided of a linear interpolation unit to generate intermediate values between consecutive encoder signal events. Capability to operates in 2 wires only.

Detailed Description

This module executes these functions:

1. Counting of the encoder phases and index capture function.
2. Evaluate rotor electric angle.
3. Create inter phases angle using interpolation,
4. Operating with 2 wires only (no index).

Each function is implemented in the IP Core with a process.

The encoder interface consists of three data signals ***incha***, ***inchb***, ***inchi*** generated by the encoder for the Channel A and Channel B (this signal are in quadrature); ***inchi*** is the encoder index signal. ***angtg*** is used to drive the interpolator for intermediate angle generations between two consecutive encoder phase events. The ***angtg*** signal is usually synchronized with FOC cycle time.

In case of 2 phase only encoder the ***inchi*** signal shall be locked to '1' or '0' and ***xmchi*** in opposite value.

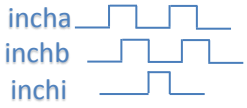

Figure 1 - encoder signals

The encode signals ***incha*** and ***inchb*** shall changes in "gray counter" sequence. At every changes the ***phase*** counter is updated (+1 or -1) according phase sequence. The new angle value is generated and the interpolator starts the speed evaluation to create inter phases angle values.

The static signal ***xmcha***, ***xmchb***, ***xmchi*** shall be set according the expected index event.

The correct value for the showed figure is ***xmcha***=0, ***xmchb***=0, ***xmchi***=1.

The encoder can operate without index as design specification or in case of runtime h/w failure.

If ***inchi*** is fixed value "0" or "1" the index event is not detected (inchi dead).

When first index event occur the ***phcnt*** and ***angle*** are both saved for reusing on successive index events.

The index events are counted in ***index*** counter.

The index events are used to synchronized the counting in case of phases loss due to h/w error or noise.

The ***fwdir*** signal indicates the direction of the encoder. If ***fwdir*** is high (logical '1') then it indicates the forward direction (main direction). The low value (logical '0') indicates reverse direction.

The ***phsev*** event indicates phase counter changing (valid transition of ***incha***, ***inchb*** signals).

The ***idxev*** event indicates the index event detection (***incha***=***xmcha*** and ***inchb***=***xmchb*** and ***inchi***=***xmchi*** and ***inchi*** alive) and then the ***index[31:0]*** output is incremented.

The ***errev*** event indicates an invalid transition of ***incha***, ***inchb*** signals (H/W problems or over speed).

PARAMETERS

Parameter	Type	Values	Default	Description
C_FAMILY	string	spartan3adsp spartan6 kintex7	spartan3adsp	Xilinx FPGA Family name

SIGNALS

Signal	I/O	Description
clock	IN	Clock (rising edge).
reset	IN	Reset the encoder. Active high.
init	IN	Secondary reset signal used to align encoder output to motor rotor position.
inten	IN	Interpolator enable (1=enable, 0=disable)
angtg	IN	Interpolator angle generation trigger
incha	IN	Encoder channel A.
inchb	IN	Encoder channel B.
inchi	IN	Encoder index pulse.
xmcha	IN	Encoder channel A value for index event detection
xmchb	IN	Encoder channel B value for index event detection
xmchi	IN	Encoder channel I value for index event detection
phsrnd[15:0]	IN	Phases per round. (cycles per revolution CPR * 4)
angdef[31:0]	IN	Default angle set when **reset** or **init** asserted. UNSIGNED32.
angphs[31:0]	IN	Set the electric angle equivalent to a step of the encoder data phase. UNSIGEND32.
fwdir	OUT	Direction of rotation (high=forward, low=reverse).
phsev	OUT	Phase encoder change event. Active high. The pulse is of 1 clock cycle. There is a pulse every time the ***cha*** or ***chb*** inputs change.
idxev	OUT	Index encoder change event. Active high. The pulse is of 1 clock cycle. There is a pulse when ***chi*** goes high.
errev	OUT	Error event. (no gray sequence in cha, chb changes)
phcnt[15:0]	OUT	Phase in round. (the value is in range 0..phsrnd-1)
phase[31:0]	OUT	Phase encoder counter. SIGNED32.
phcpt[31:0]	OUT	Phase encoder counter at the encoder index pulse event. Latched until next index pulse. SIGNED32.
angle[31:0]	OUT	Phase electrical angle. UNSIGNED32. 2^{32}=360 degree
index[31:0]	OUT	Index event counter. UNSIGNED32.

TIMING PERFORMANCE AND RESOURCE USAGE

This section provides data on the timing performance and resource utilization of the core. Performance has been obtained on one representative device from the Spartan-3 Generation and Spartan 6 families of FPGAs. The following tables lists the devices used for characterization.

Device Utilization

Device Utilization Summary (estimated values)	
Logic Utilization	**Spartan3A DSP**
Number of Slices	420
Number of Slice Flip Flops	532
Number of 4 input LUTs	637
Number of DSP48s	1

Device Utilization Summary (estimated values)	
Logic Utilization	**Spartan 6**
Number of Slice Registers	520
Number of Slice LUTs	560
Number of fully used LUT-FF pairs	354
Number of DSP48A1s	1

Device Utilization Summary (estimated values)	
Logic Utilization	**Kintex 7**
Number of Slice Registers	510
Number of Slice LUTs	541
Number of fully used LUT-FF pairs	339
Number of DSP48E1s	1

Execution time

output	input	clock cycle[1]
angle[31:0]	angtg	7
angle[31:0]	incha,inchb	42

[1] Unless otherwise noted.

Reference Documents

1. Xilinx LogiCORE IP DSP48 Macro V2.1 [DS754 March 1, 2011]

Support

QDESYS provides technical support for this LogiCORE product when used as described in the product documentation.
QDESYS cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

For information on pricing and availability of QDESYS modules and software, please contact info@qdesys.com

Revision History

Date	Version	Description
20/11/2013	1.0	Initial QDeSys release

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